



FAILURE ANALYSIS

1109 McKay Dr • San Jose, CA 95131 • Tel: (408) 904-1100

FAILURE ANALYSIS REPORT

To: SKT/ALT
From: WH Lin
Customer #: SKT/ALT
Synaptics FACR #: 017556(SN1 and SN2)
CC: Pavan Singaraju
Date: 09/29/2022

8-Discipline Format

(1) Team Formation

Product / Testing Engineering – Scott L.
Quality / Reliability / Failure Analysis – Wh L.
Application / Design Engineering – Nghia N./Robin H.
CQE – HK L.

(2) Problem Description

Background information:

SKT/ALT - 2pcs field failure, GPIO fail

#	Device	Lot #/ Date Code	Failure Mode
SN1	VS-550 A1	051AATH 191 TBGY90 00AC	GPIO fail
SN2	VS-550 A1	051AATH 191 TBGY90 00AC	GPIO fail

(3) Containment Action

N/A

(4) Root Cause Identification & Verification

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Analysis and conclusion:

SN1:

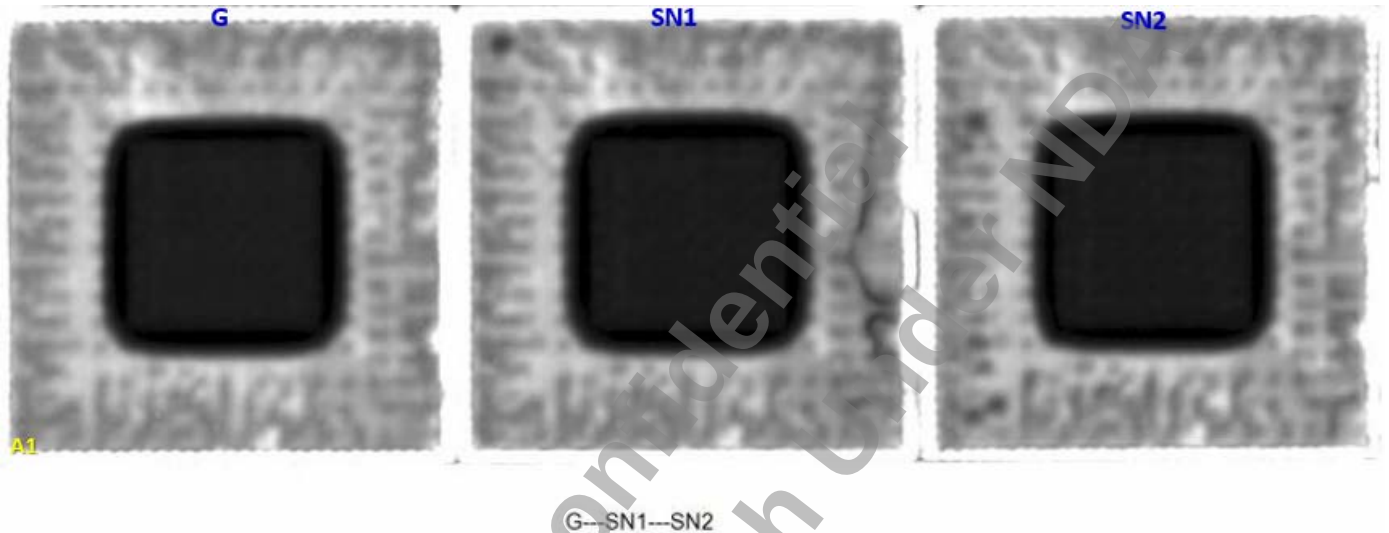
- Synaptics FA team provided non-destructive analyses for visual inspection, CSAM, and X-ray on SN1 that no abnormalities were found (Please refer to Figure 1. for visual inspection, Figure 2. for CSAM analysis and Figure 3. for X-ray analysis).



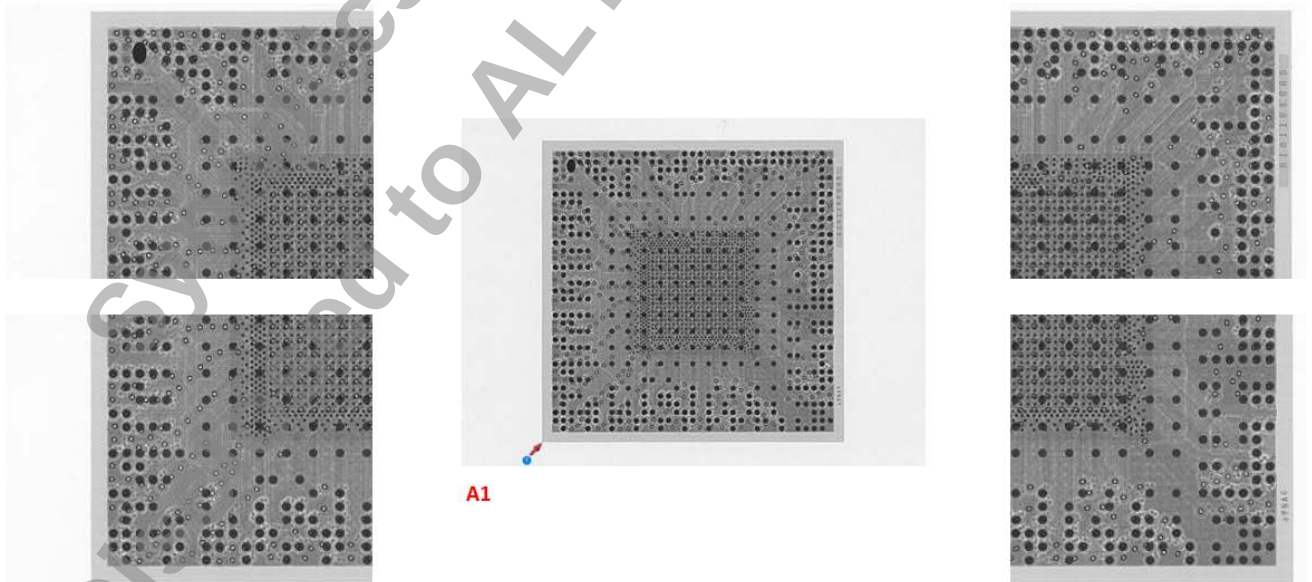
Figure 1. Visual inspection

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X-ray Analysis (SN1)



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X-ray Analysis (SN2)

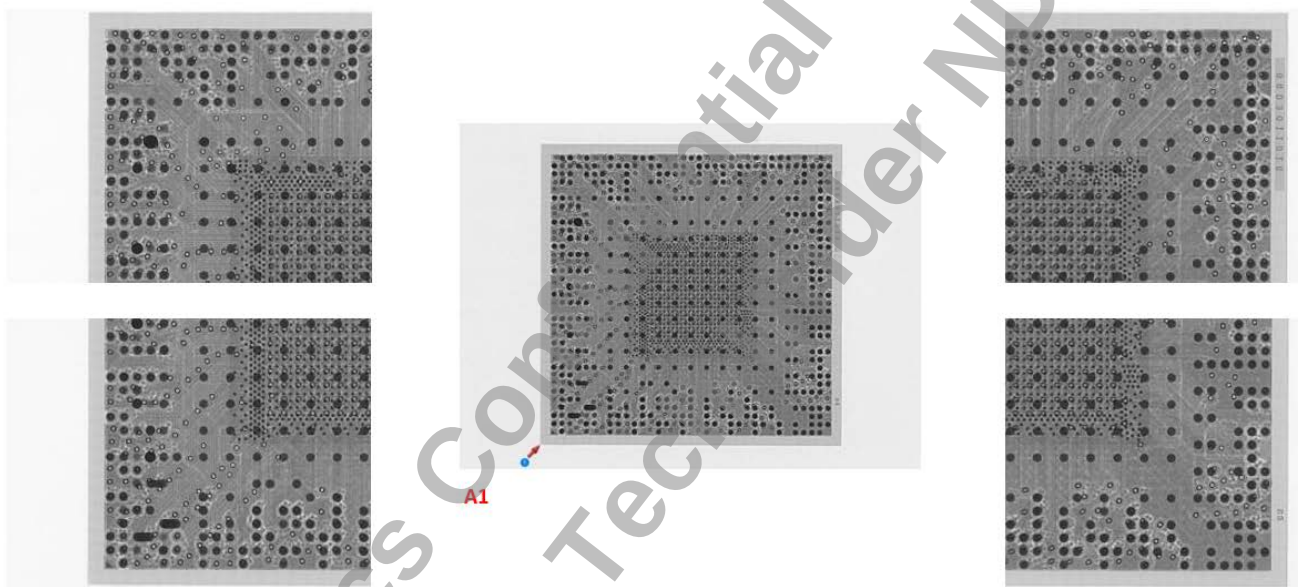


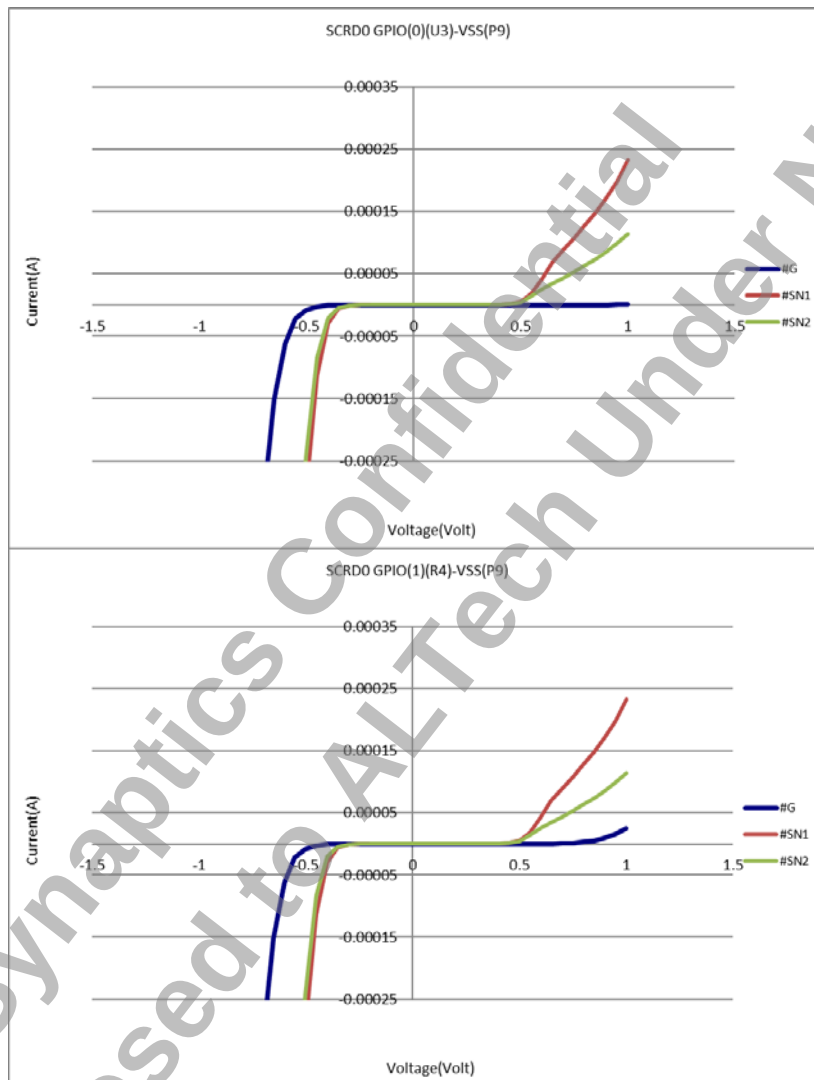
Figure 3. X-Ray analysis

- Synaptics FA team sent SN1 and SN2 to ATE with current test program that SN1 and SN2 to fail for leakage test for the pins: SCRD_GPIO[0], SCRD_GPIO[1], SDO_DAT1, SDO_DAT3, VDD_IO_6, and VDD_IO_9.
- Synaptics FA team conducted further IV curve measurement for SN1 and SN2 to check leakage failure pins shared that the leakage failure was confirmed. (Please refer to Figure 4.).



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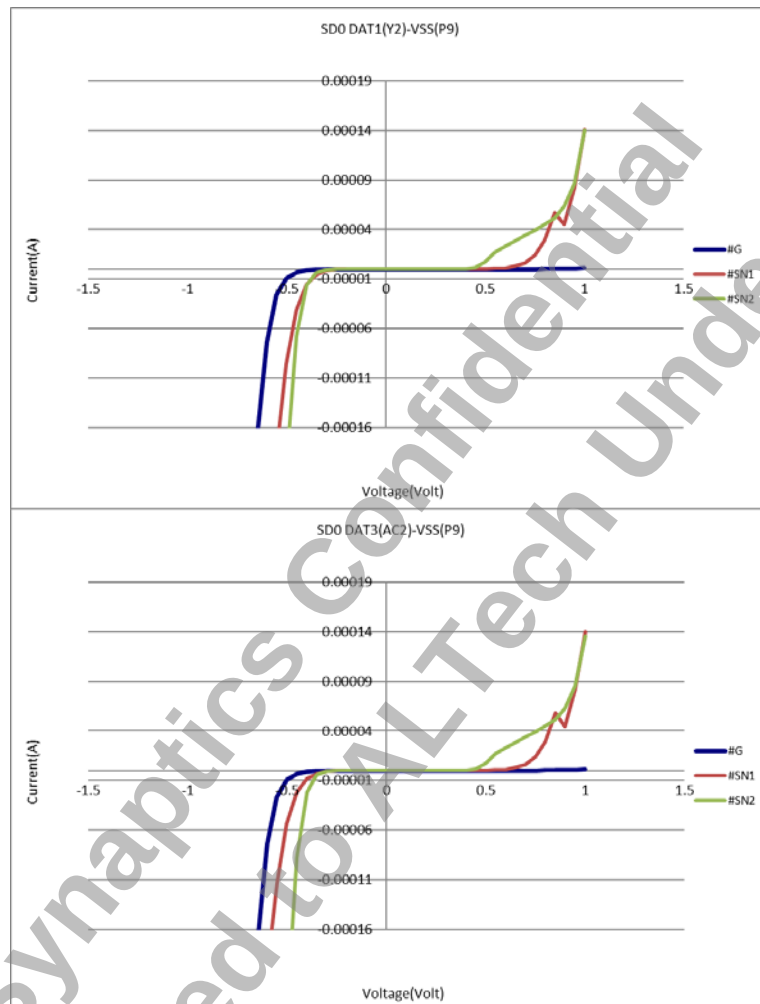
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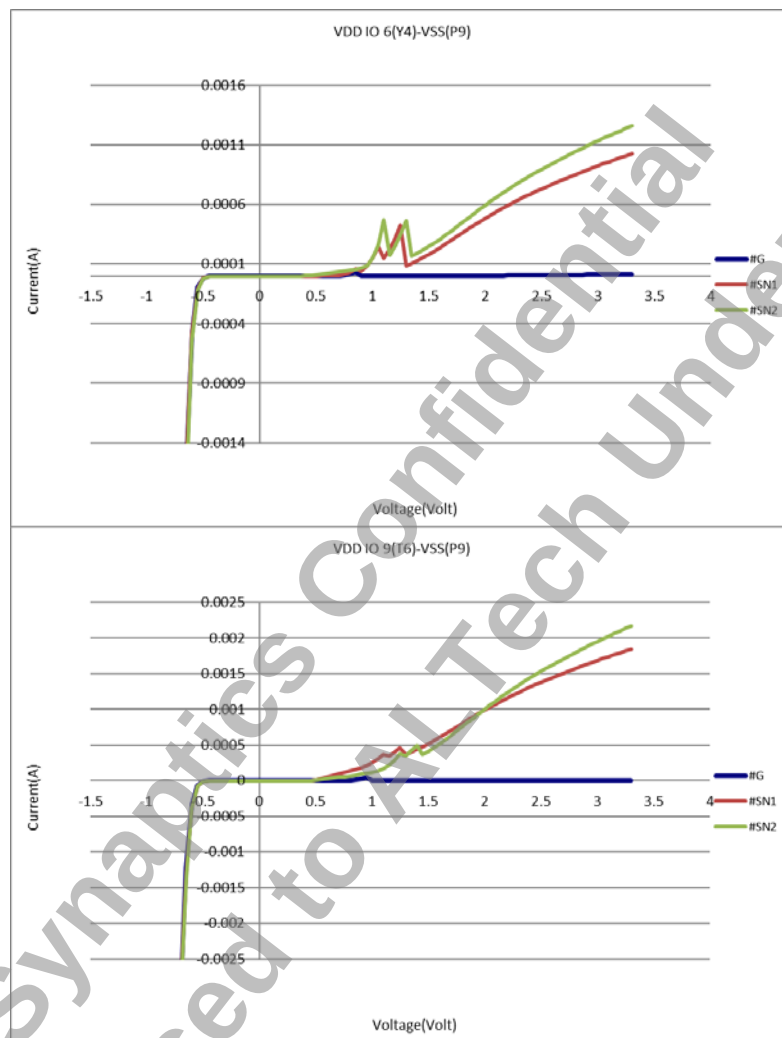
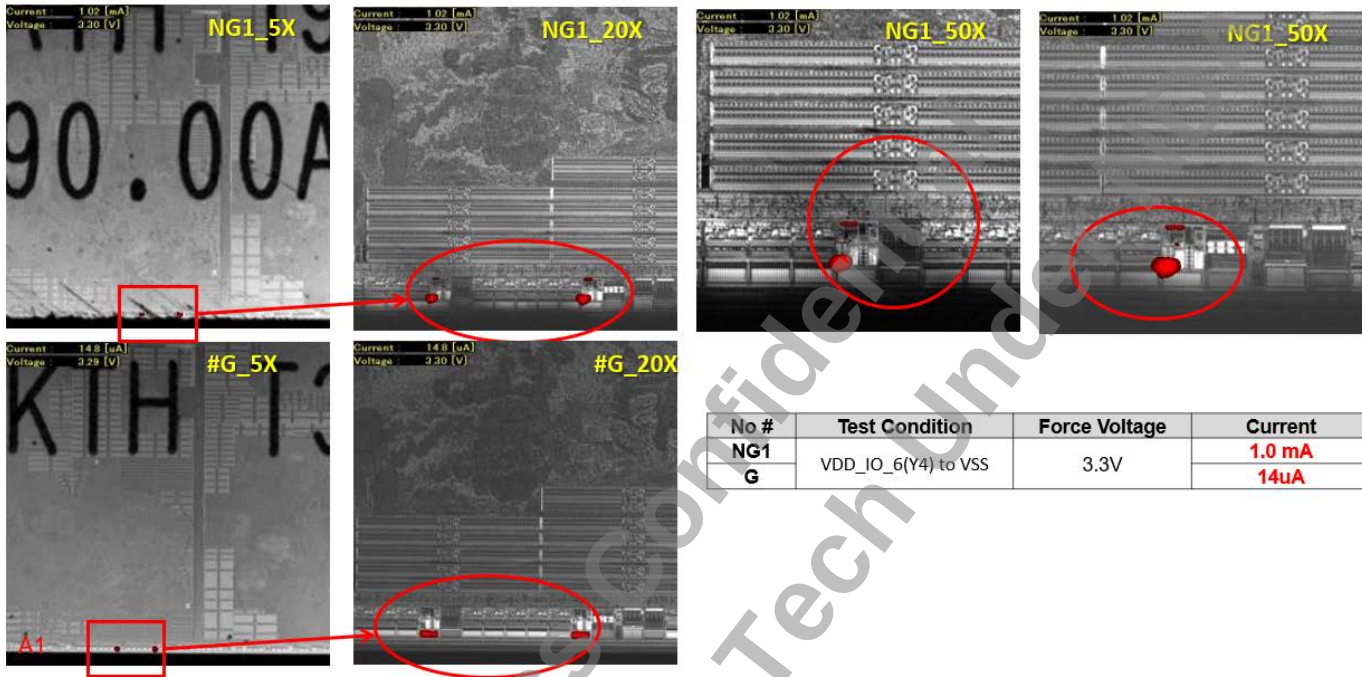


Figure 4. IV Curve analysis

- Synaptics FA team provided OBIRCH analysis for SN1 and SN2 to analyze the leakage failure pins for VDD_IO_6 and VDD_IO_9 to VSS that abnormal hot spots were found (Please refer to Figure 5.)

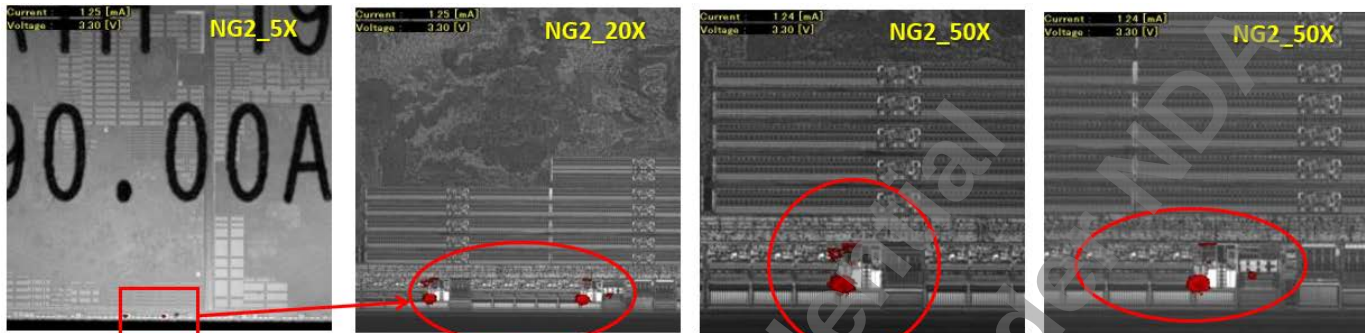
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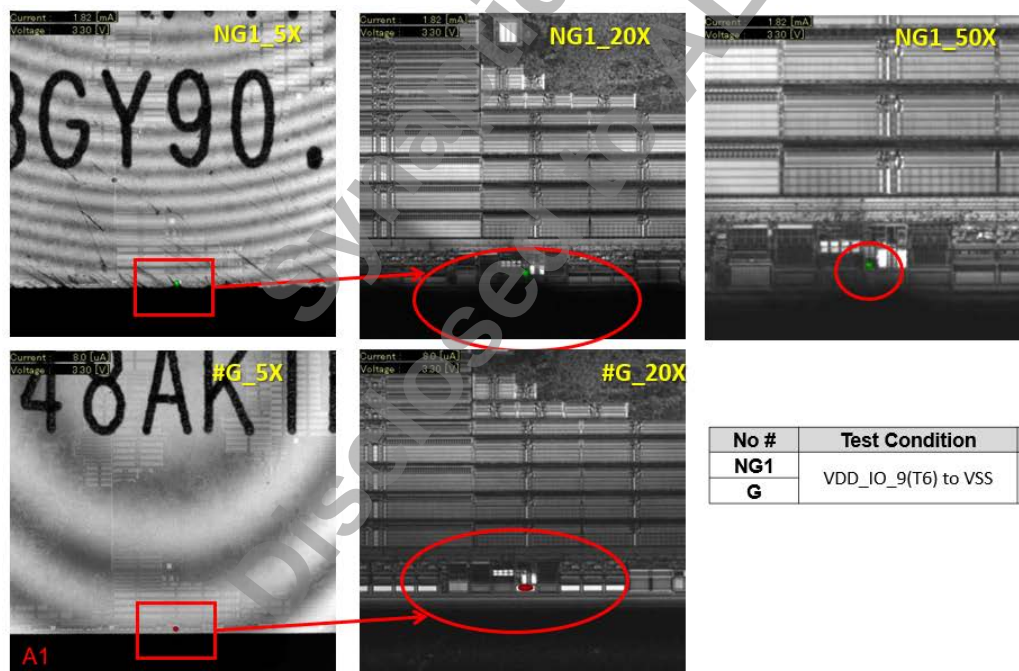


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No #	Test Condition	Force Voltage	Current
NG2 G	VDD_IO_6(Y4) to VSS	3.3V	1.0 mA
			14uA



No #	Test Condition	Force Voltage	Current
NG1 G	VDD_IO_9(T6) to VSS	3.3V	1.82 mA
			14uA

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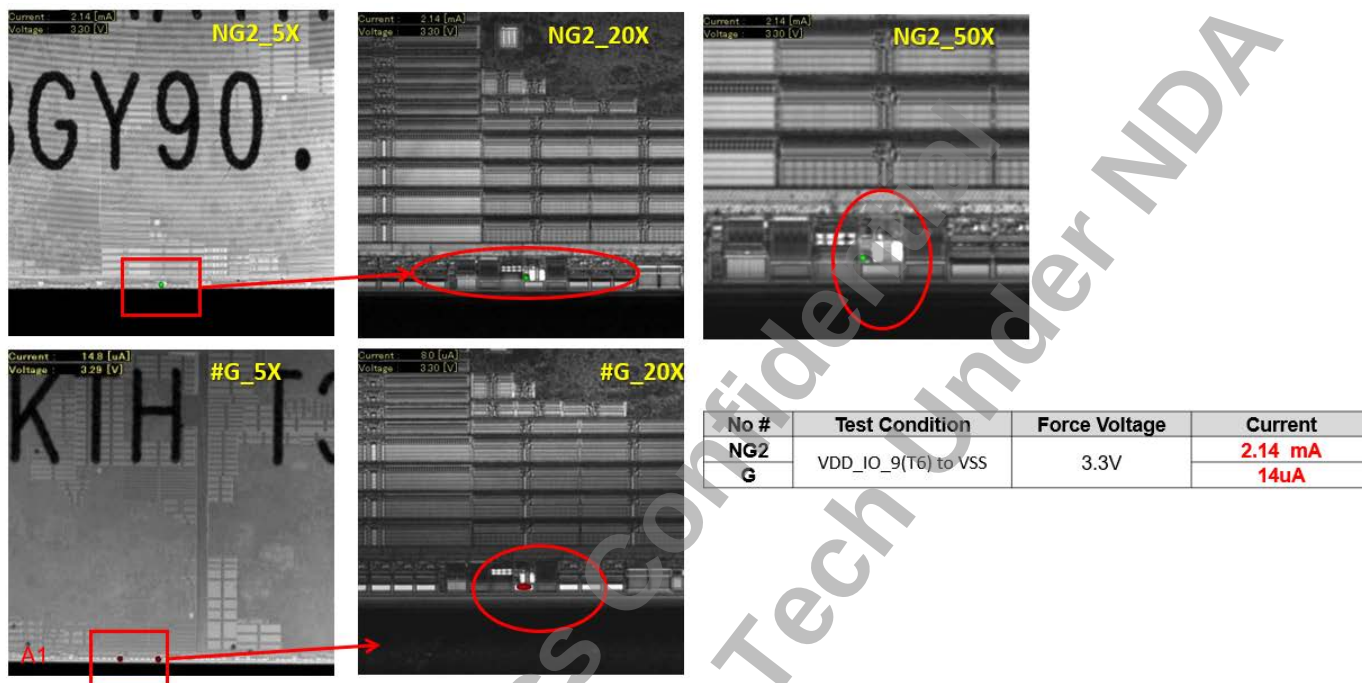


Figure 5. OBIRCH analysis

- Based on above analyses that SN1 and SN2 revealed as EOS failures from the pin for SCRD_GPIO[0], SCRD_GPIO[1], SDO_DAT1, SDO_DAT3, VDD_IO_6, and VDD_IO_9. However, we suspect the returned units of SN1 and SN2 were exposed to electrical overstress conditions. EOS occurs when a high voltage is inadvertently applied to a device for tens to several hundred milliseconds. In particular, it is important to ensure that power supplies to power pins must be clean and have good regulation. Also, it is important to ensure that the system has good signal integrity to prevent ground bounces due to abrupt variation in current consumption and over or undershoots due to transmission line reflections. Stresses beyond the recommended operating conditions may cause permanent damage.

Synaptics' devices have been extensively tested in accordance to industry's standards. A robust customer system design can help mitigate damages to its' internal components



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including Synaptics' device. Please feel free to reach out to our sales team for any applicable design guides pertinent to your Synaptics' product.

- (5) Corrective Action Plan
N/A
- (6) Implementation of Corrective Action & Verification
N/A
- (7) Preventive Action Plan
- (8) Congratulate The Team
Thank you all.

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Disclosed to ALTech Under NDA